biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor.

REMARKS/ARGUMENTS

Claim 23 has been amended by removing an unnecessary limitation. Claims 1-4, 8, 23, and 24 remain pending. Claims 1-4, 8, 23, and 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,124,741 to Arcus. All rejections are respectfully traversed.

The claimed invention relates to a charge pump circuit operated with two switching signals and their complements, e.g. UP (up), DOWN (down), $\overline{\text{UP}}$, and $\overline{\text{DOWN}}$ signals. Claim 1 defines one aspect of the invention as including, inter alia, a "first plurality of serially connected transistors", a "second plurality of serially connected transistors", where "a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal", a "gate of one of said second plurality of transistors being adapted to receive an UP pulse signal", a "first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal", and "a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal."

The subject matter of claim 1 is not disclosed in Arcus. Applicant notes that, with respect to claim 1, the Office Action identifies the Arcus Fig. 9 signals PD as